FT5506/FT5606/FT5616/FT5816

True Multi-Touch Capacitive Touch Panel Controller

INTRODUCTION

FT5506, FT5606, FT5616 and FT5816 are the single-chip capacitive touch panel controller with a built-in Micro-Controller Unit (MCU) for supporting especially large-sized mutual capacitive touch panel. They all adopt the mutual capacitance technology, which can realize true multi-touch performance. Being coupled with a mutual capacitive touch panel, FT5506/FT5606/FT5616/FT5816 can implement the user-friendly inputting function and be widely used in various portable devices in large size, such as MIDs, PADs, notebooks, tablet computer, etc.

As FT5506, FT5606, FT5616 and FT5816 are in a same series, this datasheet will present them together and list differences among them individually in the following sections.

FEATURES

- Mutual Capacitive Sensing Techniques
- True Multi-Touch with up to 10 Points of Absolute X and Y Coordinates
- Enhanced Immunity to RF Interferences and power noise
- Auto Calibration and Compensation for Environmental Variations
- FT5506 supports up to 32 TX lines + 20 RX lines without USB
- FT5606 supports up to 38 TX lines + 27 RX lines without USB
- FT5616 supports up to 38 TX lines + 27 RX lines with USB
- FT5816 Supports up to 48 TX lines + 36 RX lines with USB
- Fully Programmable Scan Sequences to Support Various TX/RX Configurations
- High Report Rate: More than 100Hz
- Capable of Driving Single Channel Resistance up to 15KΩ (including both the TX and RX lines)
- Capable of Driving Single Channel Capacitance up to 120 pF (including both the TX and RX lines)
- Optimal Sensing Mutual Capacitor for each node 1pF~4pF
- Touch Resolution up to 100 Dots per Inch (dpi) or above -- depending on the Panel Size
- 12-Bit ADC Accuracy
- Built-in Enhanced MCU
- Optional Interfaces : I^2C/SPI/USB
- External Supply Voltage 2.8V to 3.6V or USB Voltage 4.5V to 5.5V for Analog Circuits
- Built-in LDO for Digital Circuits
- IOVCC Connected to External or Internal 1.8V to 3.6V Voltage Supply for Digital IO Circuits
- 3 Operating Modes
  - Active Mode
  - Monitor Mode
  - Hibernate Mode
- Operating Temperature Range: -20°C to +85°C

TABLE OF CONTENTS

1 OVERVIEW

1.1 Typical Applications

FT5506/FT5606/FT5616/FT5816 accommodate a wide range of applications, some typical examples are listed below.

- Netbook
- Tablet PC
- Electronic Book
- MID
- PAD

FT5506/FT5606/FT5616/FT5816 support large Touch Panel, users may find out their target IC from the following table.

Model Name	Panel		Package			Touch Panel Size	USB
	TX	RX	Type	Pin	Size		
FT5506EEG	32	20	QFN	68	8x8x0.8mm	7"～8.9"	No
FT5606NED	38	27	QFN	88	10x10x0.8mm	8.9"～10.1"	No
FT5616KHD	38	27	BGA	116	8x8x0.6mm	8.9"～10.1"	Yes
FT5816KHC	48	36	BGA	116	8x8x0.6mm	>10.1"	Yes

2 FUNCTIONAL DESCRIPTION

2.1 Architectural Overview

Figure2-1 shows the overall architecture for the FT5506/FT5606/FT5616/FT5816, But FT5506/FT5606 is without USB.

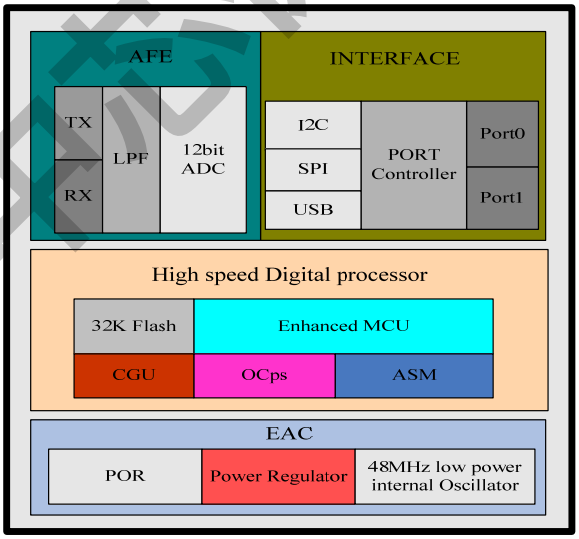


Figure 2-1 FT5506/FT5606/FT5616/FT5816 System Architecture Diagram

The FT5506/FT5606/FT5616/FT5816 is comprised of five main functional parts which are listed as below,

- Touch Panel Interface Circuits

The main function for the AFE and AFE controller is to interface with the touch panel. It scans the panel by sending AC signals to the panel and processes the received signals from the panel. So, it supports both Transmit (TX) and Receive (RX) functions. Key parameters to configure this circuit can be sent via serial interfaces, which will be explained in detail in a later section.

- Enhanced MCU

For the Enhanced MCU, larger program and data memories are supported. Furthermore, a Flash ROM is implemented to store

programs and some key parameters.
Complex signal processing algorithms are implemented with firmware running on MCU and signal process unit to detect the touches reliably. Communication protocol software is also implemented on this MCU to exchange data and control information with the host processor.

- External Interface
  - I2C/SPI/ USB: an interface for data exchange with host
  - INT: an interrupt signal to inform the host processor that touch data is ready for read
  - /RST: an external low signal reset the chip.
- A watch dog timer is implemented to ensure the robustness of the chip.
- A voltage regulator to generate 1.8V for digital circuits from the input VDD3 supply

2.2 Power Supply Selection

There are two options for power supply of FT5616/FT5816, and it is selected by PSEL pin .

- When PSEL=0, FT5616/FT5816 is powered by external Power supply, the voltage is 2.8V~3.6V, connect to VDD3 and VDDA , VBUS is connected to VDD3
- When PSEL=5V(VBUS), FT5616/FT5816 is powered by USB, the voltage is 4.5V~5.5V, connect to VBUS, VDD3 is around 3V, VDDA is Connected to VDD3.

IOVCC is 1.8~3.6V for Digital I/O, and can be connected to VDDD, VDD3 or external I/O power supply directly.

VDDD and VDD5 are provided by internal circuit.

A decoupling capacitor(1uF) must be placed between each power pin and ground.

2.3 MCU

This section describes some critical features and operations supported by the enhanced MCU.

Figure 2-2 shows the overall structure of the MCU block. In addition to the enhanced MCU core, we have added the following circuits,

- Program Memory: 32KB Flash
- Data Memory: 8KB SRAM
- Real Time Clock (RTC): A 32KHz RC Oscillator
- Timer: A number of timers are available to generate different clocks
- Master Clock: 24/ 48MHz from a 48MHz RC Oscillator or external crystal and PLL
- Clock Manager: To control various clocks under different operation conditions of the system

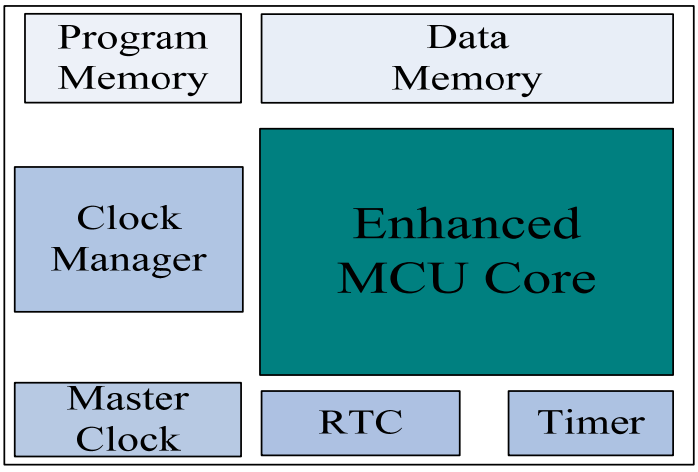


Figure 2-2 MCU Block Diagram

2.4 Operation Modes

FT5506/FT5606/FT5616/FT5816 operates in the following three modes:

- Active Mode

When in this mode, FT5506/FT5606/FT5616/FT5816 actively scans the panel. The default scan rate is 60 frames per second. The host processor can configure FT5506/FT5606/FT5616/FT5816 to speed up or to slow down.

- Monitor Mode

When in this mode, FT5506/FT5606/FT5616/FT5816 scans the panel at a reduced speed. The default scan rate is 25 frames per second and the host processor can increase or decrease this rate. When in this mode, most algorithms are stopped. A simpler algorithm is being executed to determine if there is a touch or not. When a touch is detected, FT5506/FT5606/FT5616/FT5816 shall enter the Active mode immediately to acquire the touch information quickly. During this mode, the serial port is closed and no data shall be transferred with the host processor.

- Hibernate Mode

In this mode, the chip is set in power down mode. It shall only respond to the "WAKE" or "RESET" signal from the host processor. The chip therefore consumes very little current, which help prolong the standby time for the portable devices.

2.5 Host Interface

Figure 2-3 shows the interface between a host processor and FT5506/FT5606/FT5616/FT5816. This interface consists of the following three sets of signals:

- Serial Interface
- Interrupt from FT5506/FT5606/FT5616/FT5816 to the Host
- Reset Signal from the Host to FT5506/FT5606/FT5616/FT5816

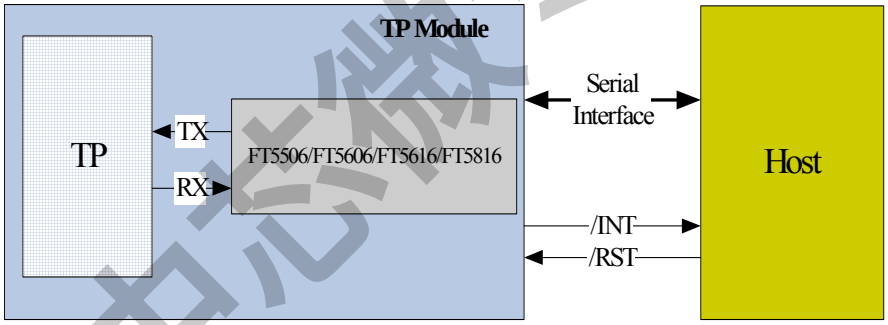


Figure 2-3 Host Interface Diagram

The serial interfaces is I2C , SPI or USB. The details of this interface are described in detail in Section **2.6**. The interrupt signal (/INT) is used for FT5506/FT5606/FT5616/FT5816 to inform the host that data are ready for the host to receive. The /RST signal is used for the host to reset FT5506/FT5606/FT5616/FT5816. After resetting, FT5506/FT5606/FT5616/FT5816 shall enter the Active mode. When the serial interface is USB, /INT and /RST are optional for FT5616/FT5816.

2.6 Serial Interface

FT5616/FT5816 supports the I2C, SPI or USB interfaces, which can be used by a host processor or other devices. FT5506/FT5606 only supports the I2C or SPI.

2.6.1 I2C

The I2C is always configured in the Slave mode. The data transfer format is shown in Figure 2-4.

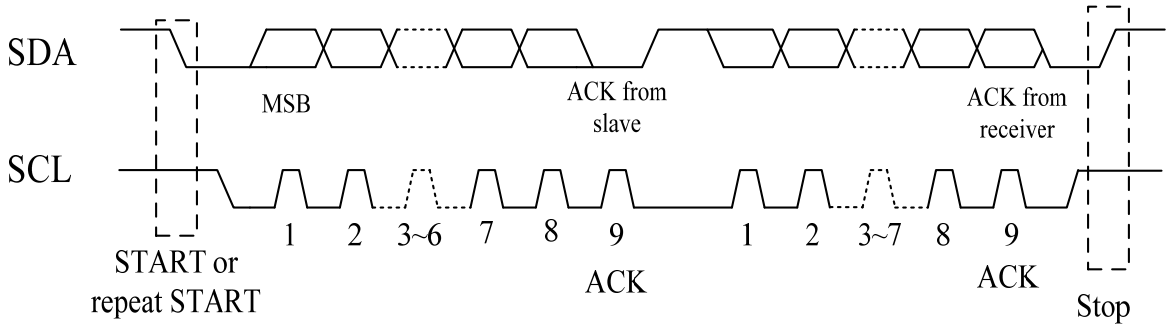


Figure 2-4 I2C Serial Data Transfer Format

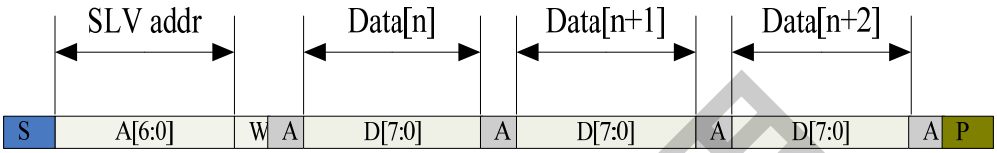


Figure 2-5 I2C master write, slave read

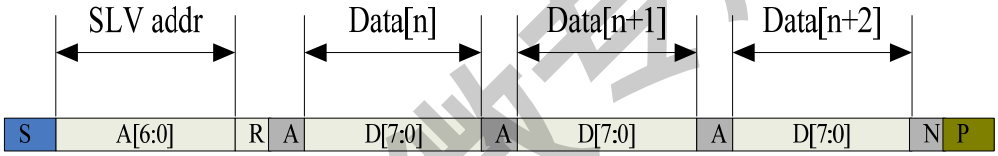


Figure 2-6 I2C master read, slave write

Table 2-1 lists the meanings of the mnemonics used in the above figures.

Table 2-1 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address A[6:4]: 3'b011 A[3:0]: data bits are identical to those of I2CCON[7:4] register.
W	1'b0: Write
R	1'b1: Read
A(N)	ACK(NACK)
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table 2-2.

Table 2-2 I2C Timing Characteristics

Parameter	Unit	Min	Max
SCL frequency	KHz	0	400
Bus free time between a STOP and START condition	us	4.7	\
Hold time (repeated) START condition	us	4.0	\

Data setup time	ns	250	\
Setup time for a repeated START condition	us	4.7	\
Setup Time for STOP condition	us	4.0	\

2.6.2 SPI

SPI is a 4 wire serial interface. The following is a list of the 4 wires:

- SCK: serial data clock
- MOSI: data line from master to slave
- MISO: data line from slave to master
- SLVESEL: active low select signal

SPI transfers data at 8bit packets. The phase relationship between the data and the clock can be defined by the two registers: phase and polck. Some data transfer examples can be found in Figure 2-7 to Figure 2-10.

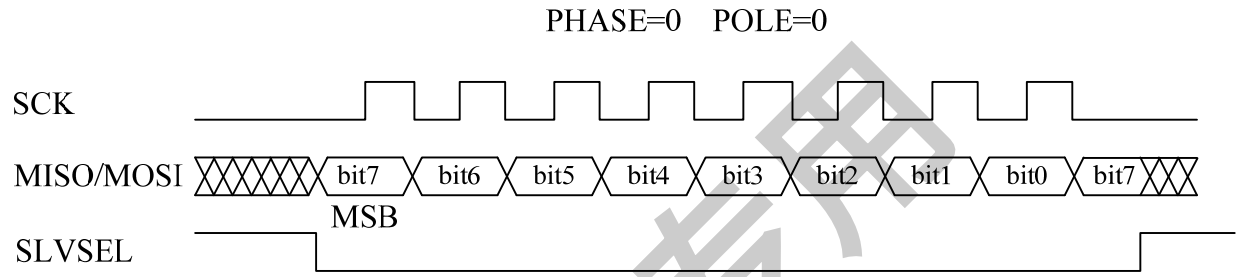


Figure 2-7 SPI Data Transfer Format (Phase=0, POLCK=0)

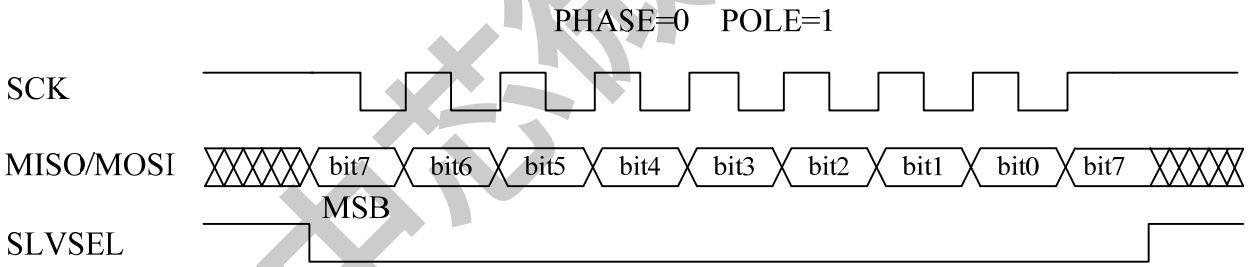


Figure 2-8 SPI Data Transfer Format (PHASE=0, POLCK=1)

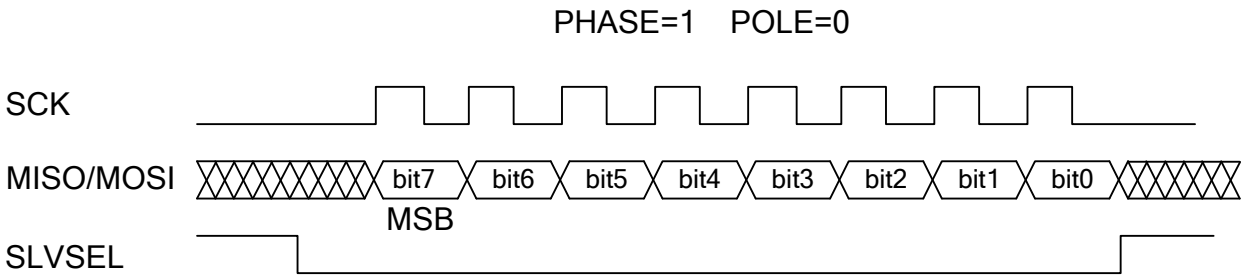


Figure 2-9 SPI Data Transfer Format (Phase=1, POLCK=0)

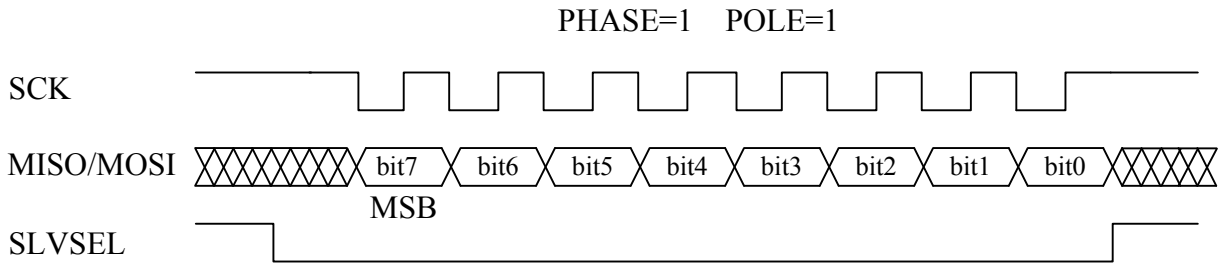


Figure 2-10 SPI Data Transfer Format (Phase=1, POLCK=1)

SPI can be configured into either Master or Slave mode via the MAS bit of the SPI0CON register. When in the Master mode, the SPI needs to supply the data clock, whose frequency relationship with the Master clock can be set by CLKDVD bits of the SPI0CON register. When it is configured in the Slave mode, the clock, SCK, is supplied by the external Master. The maximum data clock frequency must not be higher than $\frac{F_{mclk}}{8}$.

SPI Interface Timing Characteristics is shown in the following Figure2-11,Figure2-12, Figure2-13, Figure2-14 and Table 2-3.

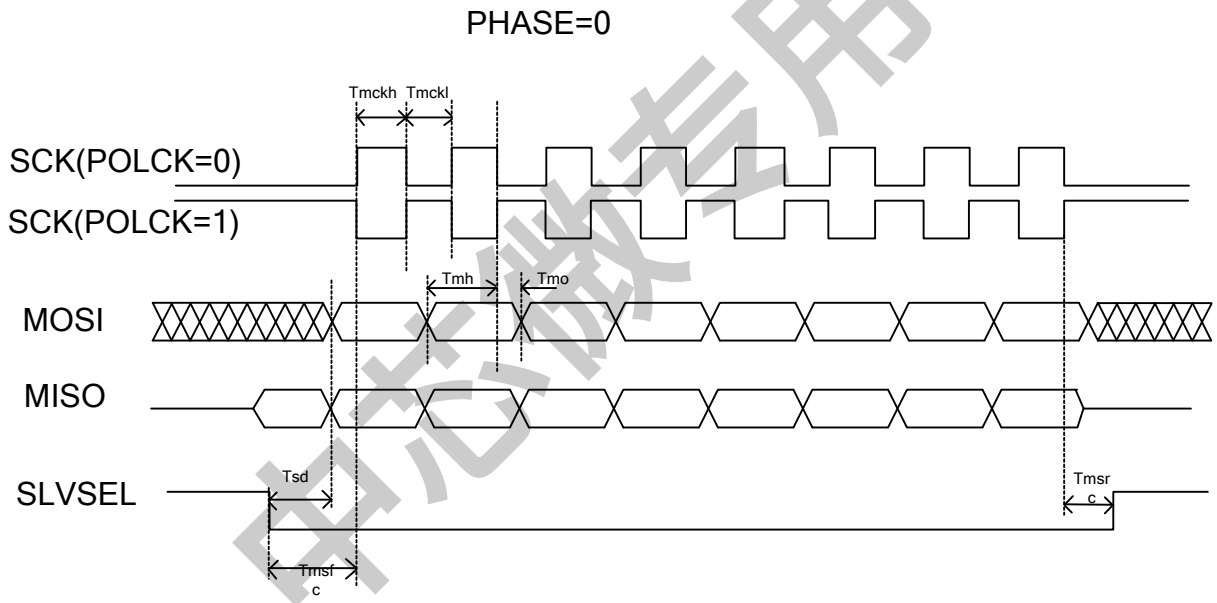


Figure 2-11 SPI master Timing PHASE =0

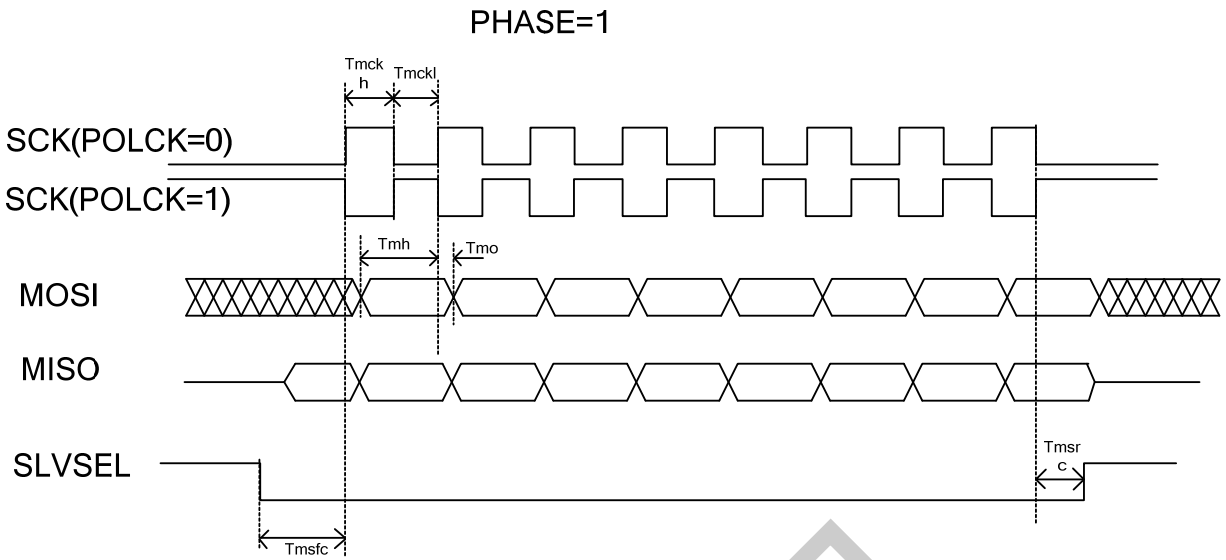


Figure 2-12 SPI master Timing PHASE =1

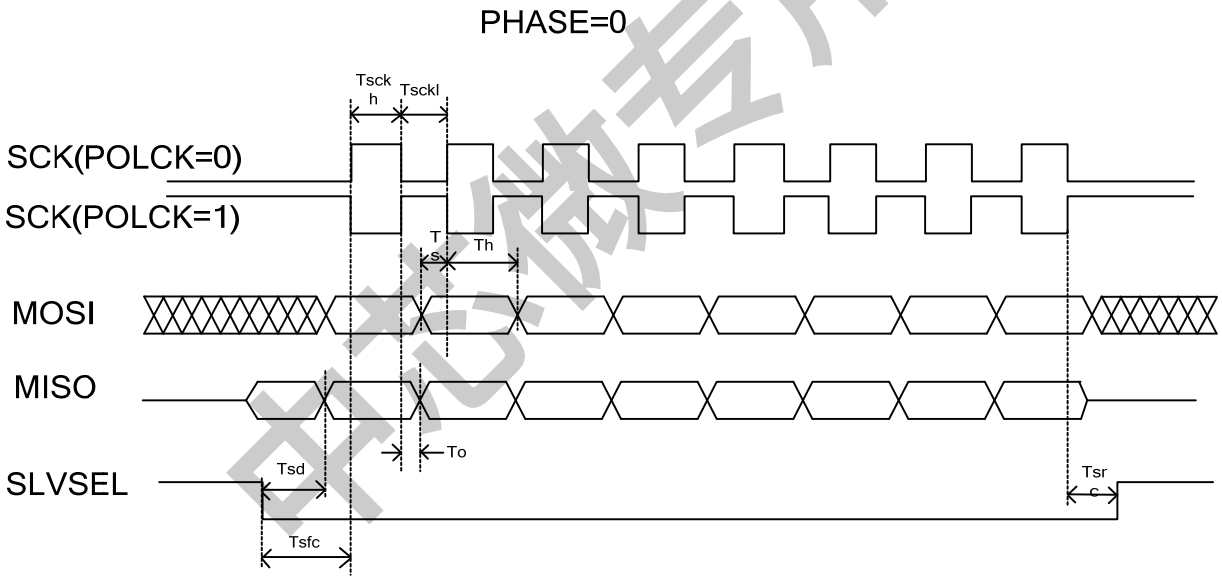


Figure 2-13 SPI slave Timing PHASE = 0

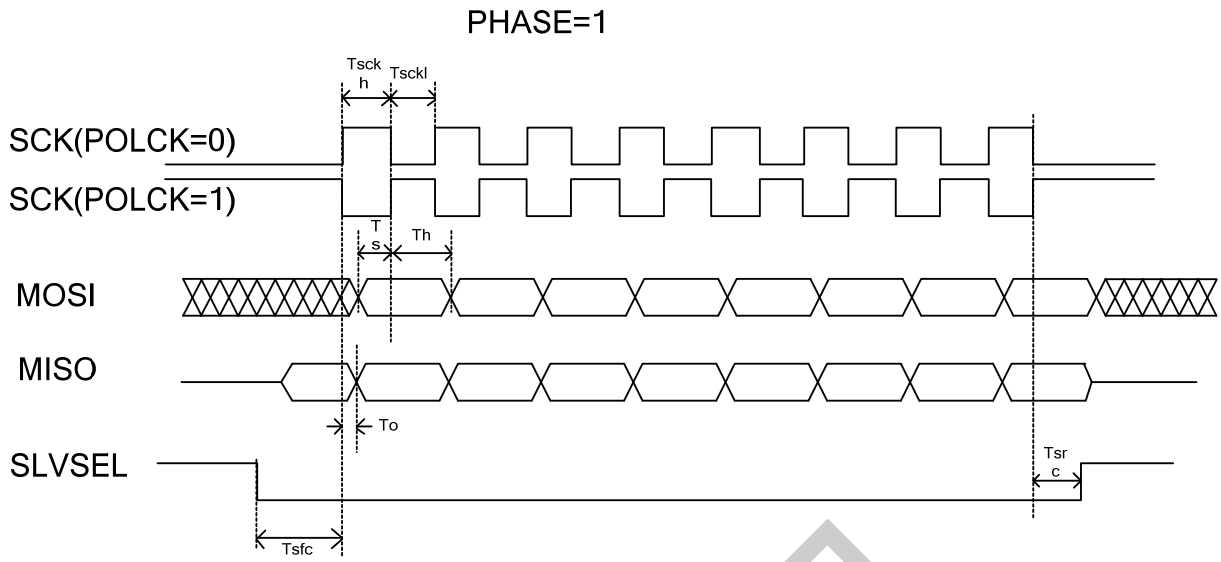


Figure 2-14 SPI slave Timing PHASE = 1

Table 2-3 SPI Timing Parameters

Parameter	Description	Min	Max	Units
Master Mode timing (see figure 2-11,2-12)				
Tmckh	sck high time	4×Tsysclk	--	ns
Tmckl	sck low time	4×Tsysclk	--	ns
Tmo	sck shift edge to mosi data change	0	--	ns
Tmh	mosi data valid to sck shift edge	3×Tsysclk	--	ns
Tsd	slvsel falling edge to mosi data valid	4×Tsysclk	--	ns
Tmsfc	slvsel falling edge to first sck edge	(Tmckh+Tmckl)/ 2	--	ns
Tmsrc	last sck edge to slvsel rising edge	(Tmckh+Tmckl)/ 2	--	ns
Slave mode timing(See figure 2-13,2-14)				
Tsckh	sck high Time	4×Tsysclk	--	ns
Tsckl	sck low Time	4×Tsysclk	--	ns
Tsd	slvsel falling edge to Miso valid data time	0	4xTsysclk	ns
Ts	Mosi Data valid to sck sample edge	0	--	ns
Th	sck sample edge to Mosi data change	4×Tsysclk	--	ns
To	sck shift edge to Miso data change	0	4xTsysclk	ns
Tsfc	slvsel falling edge to first sck edge	4×Tsysclk	--	ns
Tsrc	last sck edge to slvsel rising edge	4×Tsysclk	--	ns
*Tsysclk is equal to one period of the device system clock				

2.6.3 USB

USB is configured in device mode, and a Full speed USB function is supported. The USB function controller is as follows.

- USB specification 1.1 compliant;

- Full speed (12Mbps) ;
- Require external crystal (12MHz)for full speed ;
- Support 4 flexible endpoints;
- 1KB USB buffer memory;
- integrated transceiver;
- Support HID protocol.

3 ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Item	Symbol	Unit	Value	Note
Power Supply Voltage 1	VDDA - VSSA	V	-0.3 ~ +3.6	1, 2
Power Supply Voltage 2	VDD3 – VSS	V	-0.3 ~ +3.6	1, 3
USB Supply Voltage	VBUS	V	4.5~5.5	1
I/O Digital Voltage	IOVCC	V	1.8~3.6	1
Operating Temperature	Topr	℃	-20 ~ +85	1
Storage Temperature	Tstg	℃	-55 ~ +150	1

Notes
1.If used beyond the absolute maximum ratings, FT5506/FT5606/FT5616/FT5816 may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.
2.Make sure VDDA(high)≥VSSA (low)
3.Make sure VDD (high)≥VSS (low)

3.2 DC Characteristics

Table 3-2 DC Characteristics (VDDA=VDD3=2.8~3.6V, Ta=-20~85℃)

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high-level voltage	VIH	V		0.7 x IOVCC	--	IOVCC	
Input low -level voltage	VIL	V		-0.3	--	0.3 x IOVCC	
Output high -level voltage	VOH	V	IOH=-0.1mA	0.7 x IOVCC	--	--	
Output low -level voltage	VOL	V	IOH=0.1mA	--	--	0.3 x IOVCC	
I/O leakage current	ILI	μA	Vin=0~VDDA	-1	--	1	
Current consumption （Normal operation mode）	Iopr	mA	VDDA=VDD3 = 2.8V Ta=25℃ MCLK=24MHz	--	15	--	
Current consumption （Monitor mode）	Imon	mA	VDDA=VDD3 = 2.8V Ta=25℃ MCLK=24MHz	--	8	--	
Current consumption （Sleep mode）	Islp	μA	VDDA=VDD3 = 2.8V Ta=25℃ MCLK=24MHz	--	30	--	
Step-up output voltage	VDD5	V	VDDA=VDD3= 2.8V	4.5	5.25	5.5	
Power Supply voltage	VDDA VDD3	V		2.8		3.6	

3.3 AC Characteristics

Table 3-3 AC Characteristics of Oscillators

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
OSC clock 1	fosc1	MHz	VDD3 = 2.8V Ta=25℃	43	48	52	
OSC clock 2	fosc2	KHz	VDD3 = 2.8V Ta=25℃	29	32	36	
PLL clock	Pclk	MHz	VDD3 = 2.8V Ta=25℃	-	48	-	
Crystal clock	Cclk	MHz	VDD3 = 2.8V Ta=25℃	-	12	-	

Table 3-4 AC Characteristics of TX & RX

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Note
TX acceptable clock	ftx	KHz		100	150	270	
TX output rise time	Ttxr	nS		--	20	--	
TX output fall time	Ttxf	nS		--	20	--	
RX input voltage	Trxi	V		1.2	--	1.6	

3.4 I/O Ports Circuits

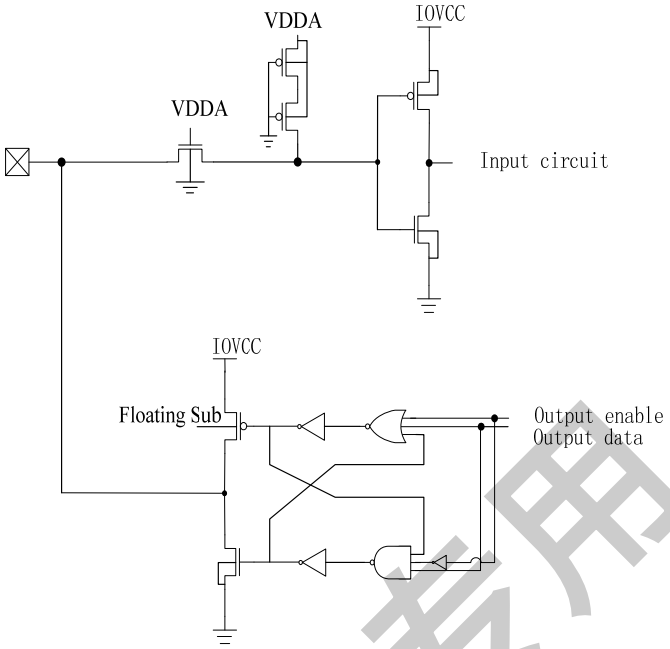


Figure 3-1 Digital In/Out Port Circuit

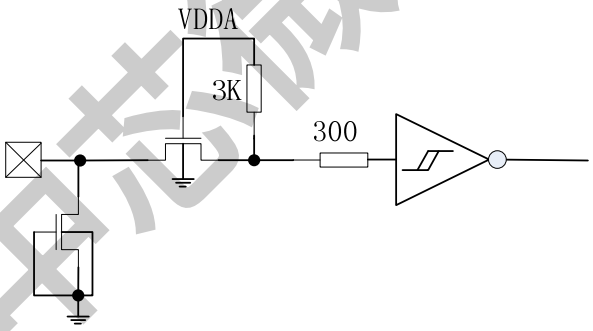


Figure 3-2 Reset Input Port Circuits

3.5 POWER ON/Reset/Wake Sequence

Reset should be pulled down to be low before powering on and powering down. I2C/SPI shouldn't be used by other devices during Reset time after IOVCC powering on (Tprt). INT signal will be sent to the host after initializing all parameters and then start to report points to the host.

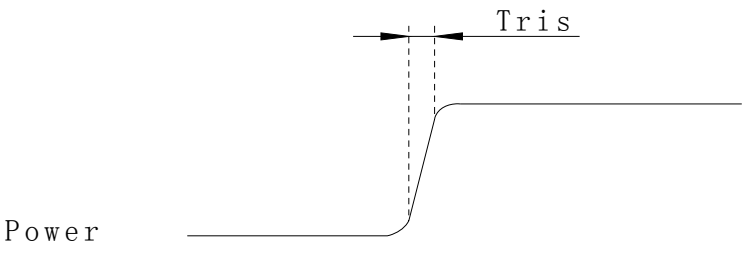


Figure 3-7 Power on time

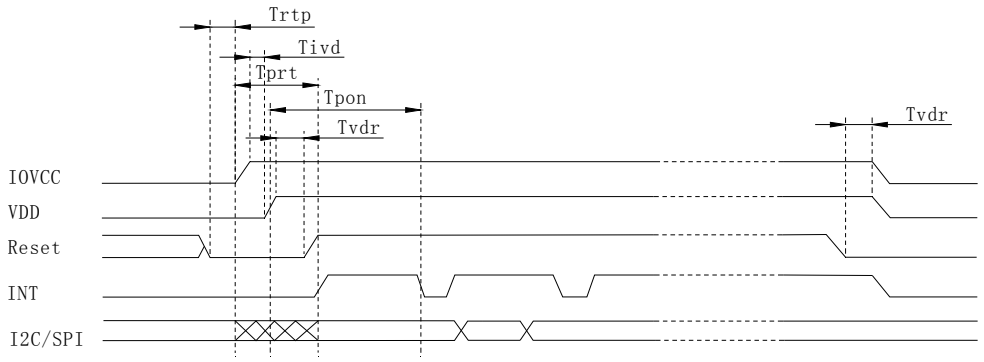


Figure 3-8 Power on / down Sequence

Reset time must be enough to guarantee reliable reset, The time of starting to report point after resetting approach to the time of starting to report point after powering on.

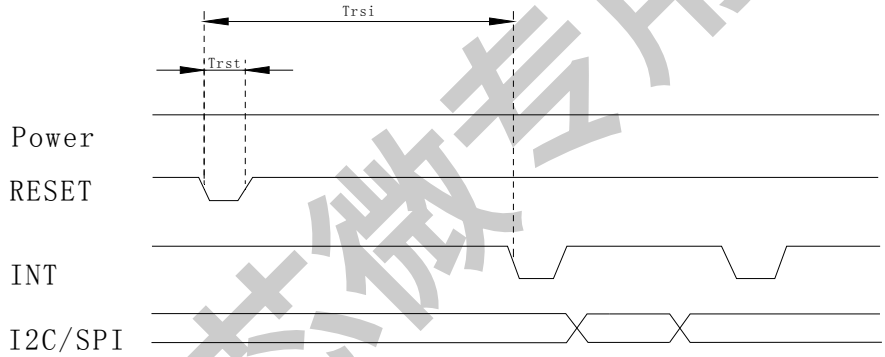


Figure 3-8 Reset Sequence

Table 3-5 Power on/Reset/Wake Sequence Parameters

Parameter	Description	Min	Max	Units
Tris	Rise time from 0.1VDD to 0.9VDD	--	5	ms
Trtp	Time of resetting to be low before powering on	100	--	μs
Tivd	Delay time of VDD powering on after IOVCC powering on	10	--	μs
Tprt	Reset time after IOVCC powering on	2Tris+Tivd+Tvdr	--	ms
Tpon	Time of starting to report point after powering on	400	--	ms
Tvdr	Reset time after VDD powering on	1	--	ms
Trsi	Time of starting to report point after resetting	400	--	ms
Trst	Reset time	1	--	ms

4 PIN CONFIGURATIONS

Pin List of FT5506EEG/FT5606NED/FT5616KHD/FT5816KHC

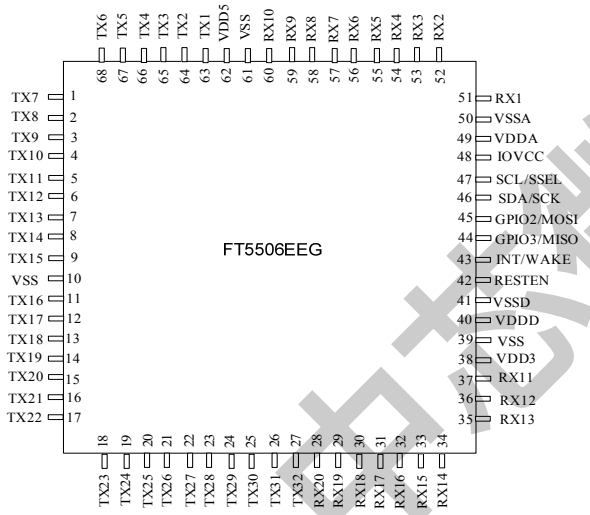
Table 4-1 Pin Definition of FT5506EEG/FT5606NED/FT5616KHD/FT5816KHC

Name	Pin No.				Type	Description
	FT5506EEG	FT5606NED	FT5616KHD	FT5816KHC		
TX48			G7	G7	O	Transmit output pin
TX47			G8	G8	O	Transmit output pin
TX46			H8	H8	O	Transmit output pin
TX45			H11	H11	O	Transmit output pin
TX44			H10	H10	O	Transmit output pin
TX43			H9	H9	O	Transmit output pin
TX42			I11	I11	O	Transmit output pin
TX41			J11	J11	O	Transmit output pin
TX40			K11	K11	O	Transmit output pin
TX39			I10	I10	O	Transmit output pin
TX38		32		J10	O	Transmit output pin
TX37		31		K10	O	Transmit output pin
TX36		30		I9	O	Transmit output pin
TX35		29		J9	O	Transmit output pin
TX34		28		K9	O	Transmit output pin
TX33		27	I8	I8	O	Transmit output pin
TX32	27	26	J8	J8	O	Transmit output pin
TX31	26	25	K8	K8	O	Transmit output pin
TX30	25	24	I7	I7	O	Transmit output pin
TX29	24	23	J7	J7	O	Transmit output pin
TX28	23	22	K7	K7	O	Transmit output pin
TX27	22	21	H7	H7	O	Transmit output pin
TX26	21	20	H6	H6	O	Transmit output pin
TX25	20	19	K6	K6	O	Transmit output pin
TX24	19	18	J6	J6	O	Transmit output pin
TX23	18	17	I6	I6	O	Transmit output pin
TX22	17	16	K5	K5	O	Transmit output pin
TX21	16	15	J5	J5	O	Transmit output pin
TX20	15	14	I5	I5	O	Transmit output pin
TX19	14	13	K4	K4	O	Transmit output pin
TX18	13	11	J4	J4	O	Transmit output pin
TX17	12	10	I4	I4	O	Transmit output pin
TX16	11	9	K3	K3	O	Transmit output pin
TX15	9	8	K2	K2	O	Transmit output pin
TX14	8	7	K1	K1	O	Transmit output pin
TX13	7	6	J3	J3	O	Transmit output pin
TX12	6	5		J2	O	Transmit output pin
TX11	5	4		J1	O	Transmit output pin
TX10	4	3		I3	O	Transmit output pin
TX9	3	2		I2	O	Transmit output pin

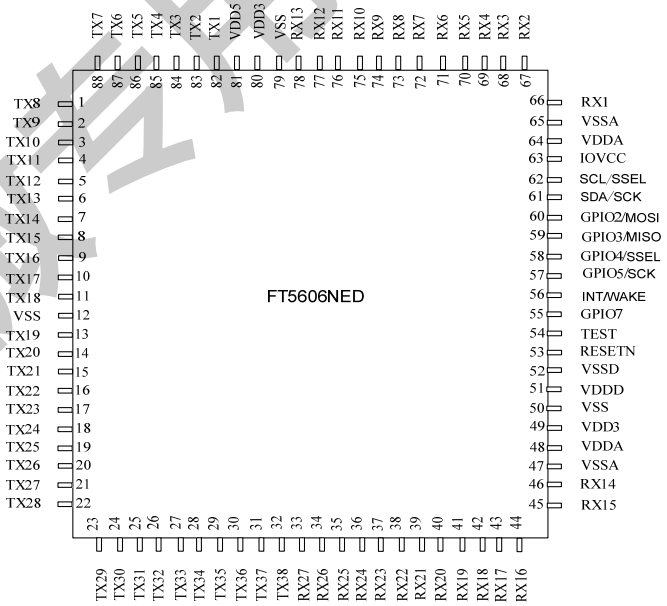
TX8	2	1		I1	O	Transmit output pin
TX7	1	88	H3	H3	O	Transmit output pin
TX6	68	87	H2	H2	O	Transmit output pin
TX5	67	86	H1	H1	O	Transmit output pin
TX4	66	85	H4	H4	O	Transmit output pin
TX3	65	84	H5	H5	O	Transmit output pin
TX2	64	83	G5	G5	O	Transmit output pin
TX1	63	82	E5	E5	O	Transmit output pin
VBUS			G1	G1	PWR	VBUS sensor input, The pin should be connected to USB 4.5~5.5V power supply. This pin must be floating or connected to VDD3 when USB Power is not adopted. A 1 μF ceramic capacitor to ground is required.
PSEL			G2	G2	I	Power Select pin. PSEL=0, powered by external voltage supply; PSEL=5V, powered by USB
VDD5	62	81	G3	G3	PWR	internal generated 5V power supply， A 1 μF ceramic capacitor to ground is required.
TEST		54	G4	G4	I	Test pin , should be tie to ground
VDDD		51	G9	G9	PWR	Digital power supply (1.8V), generated internal. A 1 μF ceramic capacitor to ground is required.
VSSD		52	G10	G10	PWR	Digital ground
VSS	61	50	G11	G11	PWR	Analog ground
VSS	39	12	F4	F4	PWR	Analog ground
VDD3	38	49	F8	F8	PWR	Analog power supply
VSS	10		E4	E4	PWR	Analog ground
VDDA	49	48	E8	E8	PWR	Analog power supply
VSSA	50	47	D4	D4	PWR	Analog ground
VSSA		65	D8	D8	PWR	Analog ground
SCL/SSEL	47	62	A5	A5	I/O	I2C clock input / SPI Slave mode, chip select, active low
SDA/SCK	46	61	A6	A6	I/O	I2C data input and output / SPI Slave mode, clock input
GPIO2/MOSI	45	60	D5	D5	I/O	General Purpose Input/Output port / SPI Slave mode, data input
GPIO3/MISO	44	59	D6	D6	I/O	General Purpose Input/Output port / SPI Slave mode, data output
GPIO4/SSEL		58	D7	D7	I/O	General Purpose Input/Output port / SPI Slave mode, chip select, active low
GPIO5/SCK		57	E7	E7	I/O	General Purpose Input/Output port / SPI Slave mode, clock input
INT/WAKE	43	56	B6	B6	I/O	External interrupt to the host / External interrupt from the host
GPIO7		55	A7	A7	I/O	General Purpose Input/Output port
RESTEN	42	53	C6	C6	I	External Reset, Low is active
VDD3		80	C4	C4	PWR	Analog power supply
VSSD	41		C8	C8	PWR	Digital ground
D-			C5	C5	I/O	USB D-
D+			B5	B5	I/O	USB D+
XN			C7	C7	I	External Clock Input
XP			B7	B7	O	External Clock Output
VDDA		64	B4	B4	PWR	Analog power supply
VSS		79	B8	B8	PWR	Analog ground

IOVCC	48	63	A4	A4	PWR	I/O power supply
VDDD	40		A8	A8	PWR	Digital power supply (1.8V), generated internal. A 1 μ F ceramic capacitor to ground is required.
NC			A1			Not connected
NC			A2			Not connected
NC			A3			Not connected
NC			B2			Not connected
NC			B3			Not connected
NC			F9			Not connected
NC			F10			Not connected
NC			F11			Not connected
NC			G11			Not connected
NC			I1			Not connected
NC			I2			Not connected
NC			I3			Not connected
NC			I9			Not connected
NC			J1			Not connected
NC			J2			Not connected
NC			J9			Not connected
NC			J10			Not connected
NC			K9			Not connected
NC			K10			Not connected
RX1	51	66		A3	I	Receiver input pins
RX2	52	67		A2	I	Receiver input pins
RX3	53	68		A1	I	Receiver input pins
RX4	54	69		B3	I	Receiver input pins
RX5	55	70		B2	I	Receiver input pins
RX6	56	71	B1	B1	I	Receiver input pins
RX7	57	72	C3	C3	I	Receiver input pins
RX8	58	73	C2	C2	I	Receiver input pins
RX9	59	74	C1	C1	I	Receiver input pins
RX10	60	75	D3	D3	I	Receiver input pins
RX11	37	76	D2	D2	I	Receiver input pins
RX12	36	77	D1	D1	I	Receiver input pins
RX13	35	78	E3	E3	I	Receiver input pins
RX14	34	46	E2	E2	I	Receiver input pins
RX15	33	45	E1	E1	I	Receiver input pins
RX16	32	44	F3	F3	I	Receiver input pins
RX17	31	43	F2	F2	I	Receiver input pins
RX18	30	42	F1	F1	I	Receiver input pins
RX19	29	41	A9	A9	I	Receiver input pins
RX20	28	40	A10	A10	I	Receiver input pins
RX21		39	A11	A11	I	Receiver input pins
RX22		38	B9	B9	I	Receiver input pins
RX23		37	B10	B10	I	Receiver input pins
RX24		36	B11	B11	I	Receiver input pins

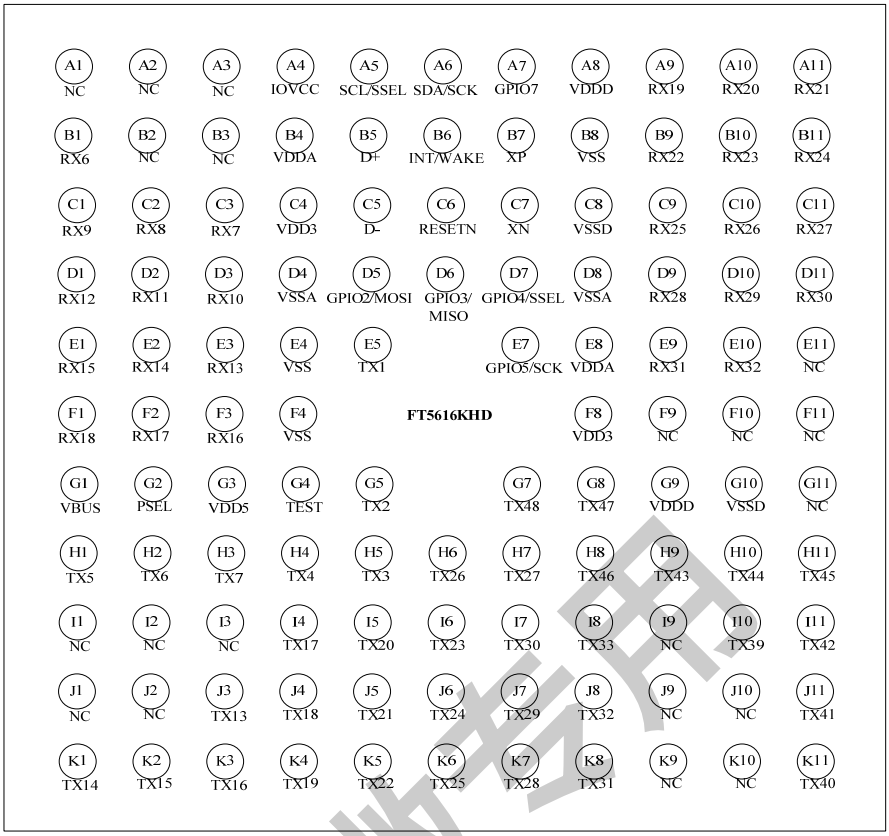
RX25		35	C9	C9	I	Receiver input pins
RX26		34	C10	C10	I	Receiver input pins
RX27		33	C11	C11	I	Receiver input pins
RX28			D9	D9	I	Receiver input pins
RX29			D10	D10	I	Receiver input pins
RX30			D11	D11	I	Receiver input pins
RX31			E9	E9	I	Receiver input pins
RX32			E10	E10	I	Receiver input pins
RX33				E11	I	Receiver input pins
RX34				F9	I	Receiver input pins
RX35				F10	I	Receiver input pins
RX36				F11	I	Receiver input pins



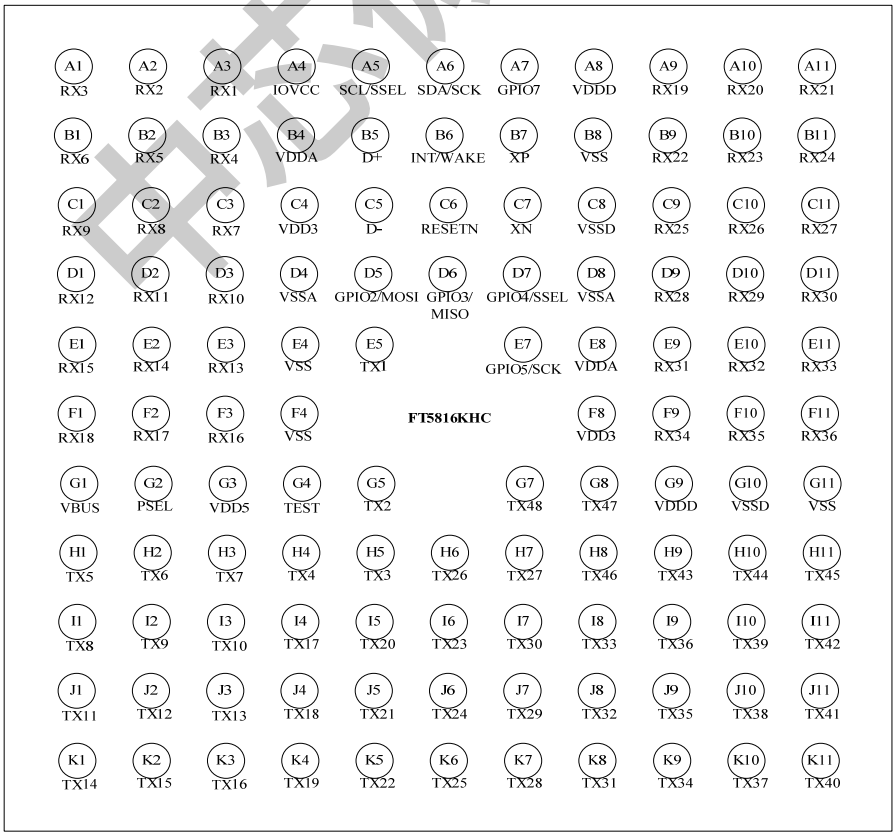
FT5506EEG Package Diagram



FT5606NED Package Diagram



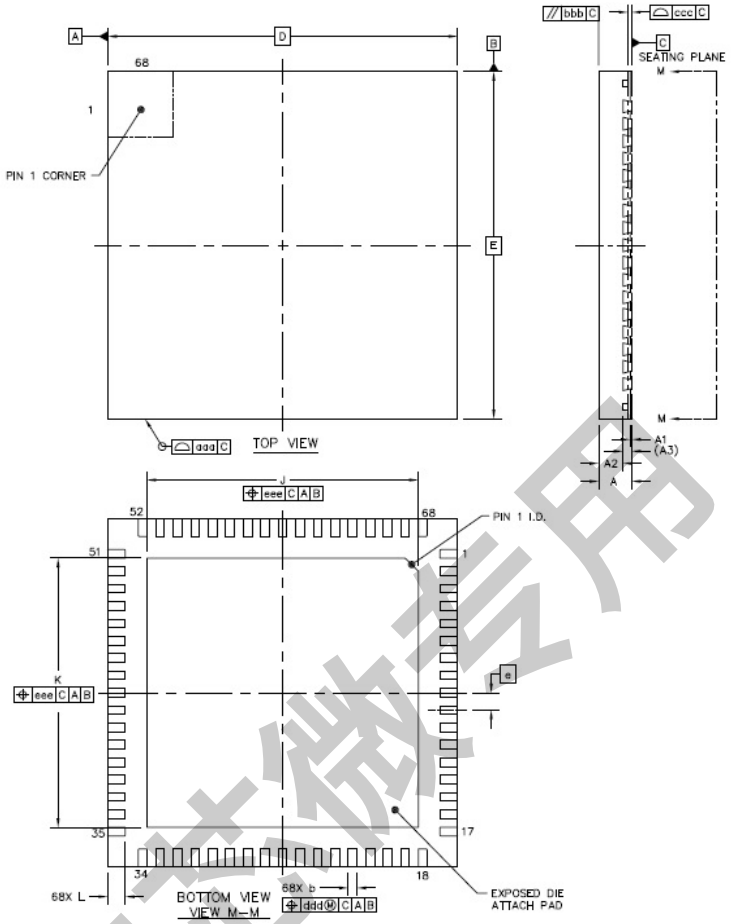
FT5616KHD Package Diagram



FT5816KHC Package Diagram

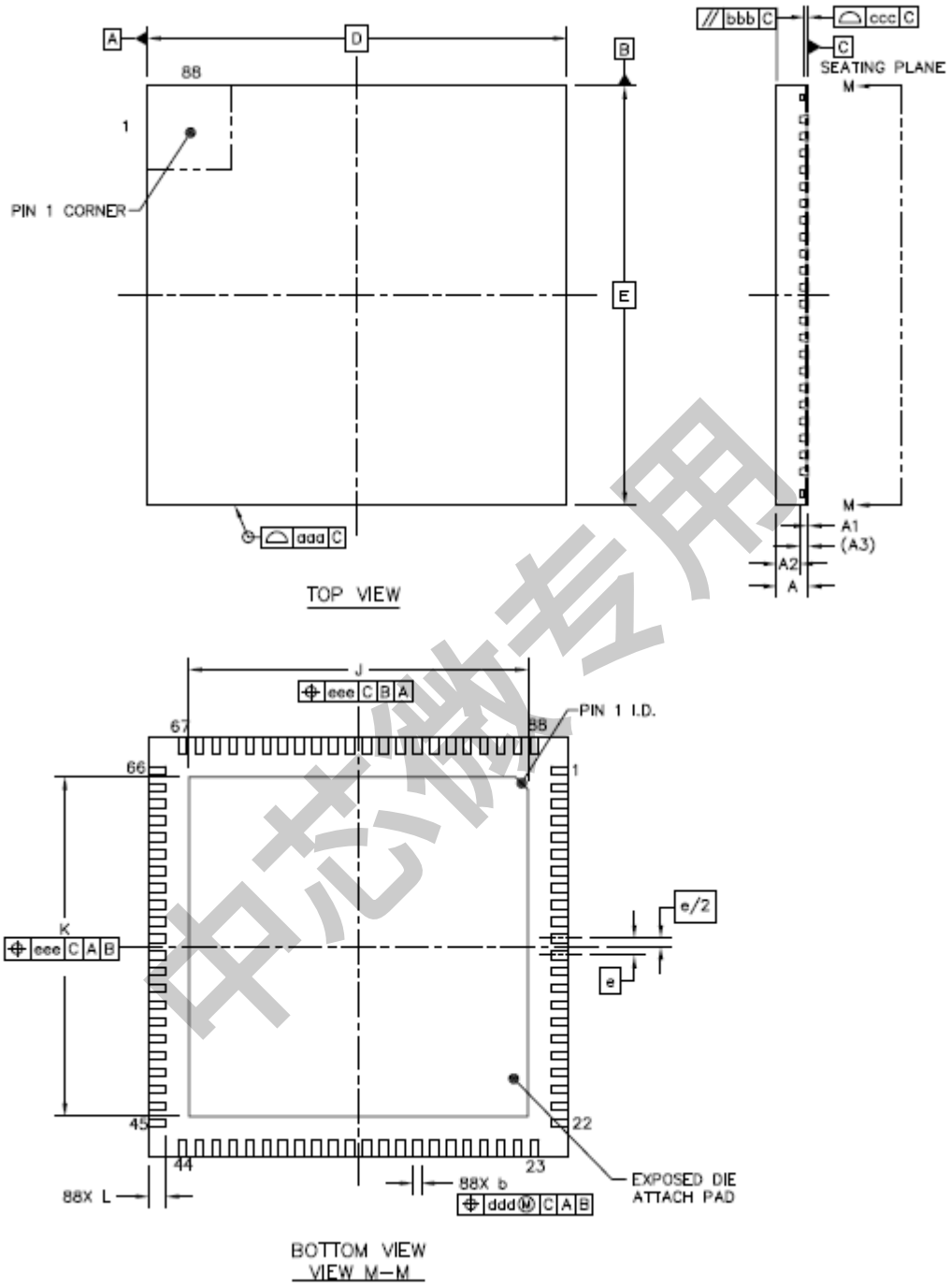
5 PACKAGE INFORMATION

5.1 Package Information of QFN-8x8-68L Package



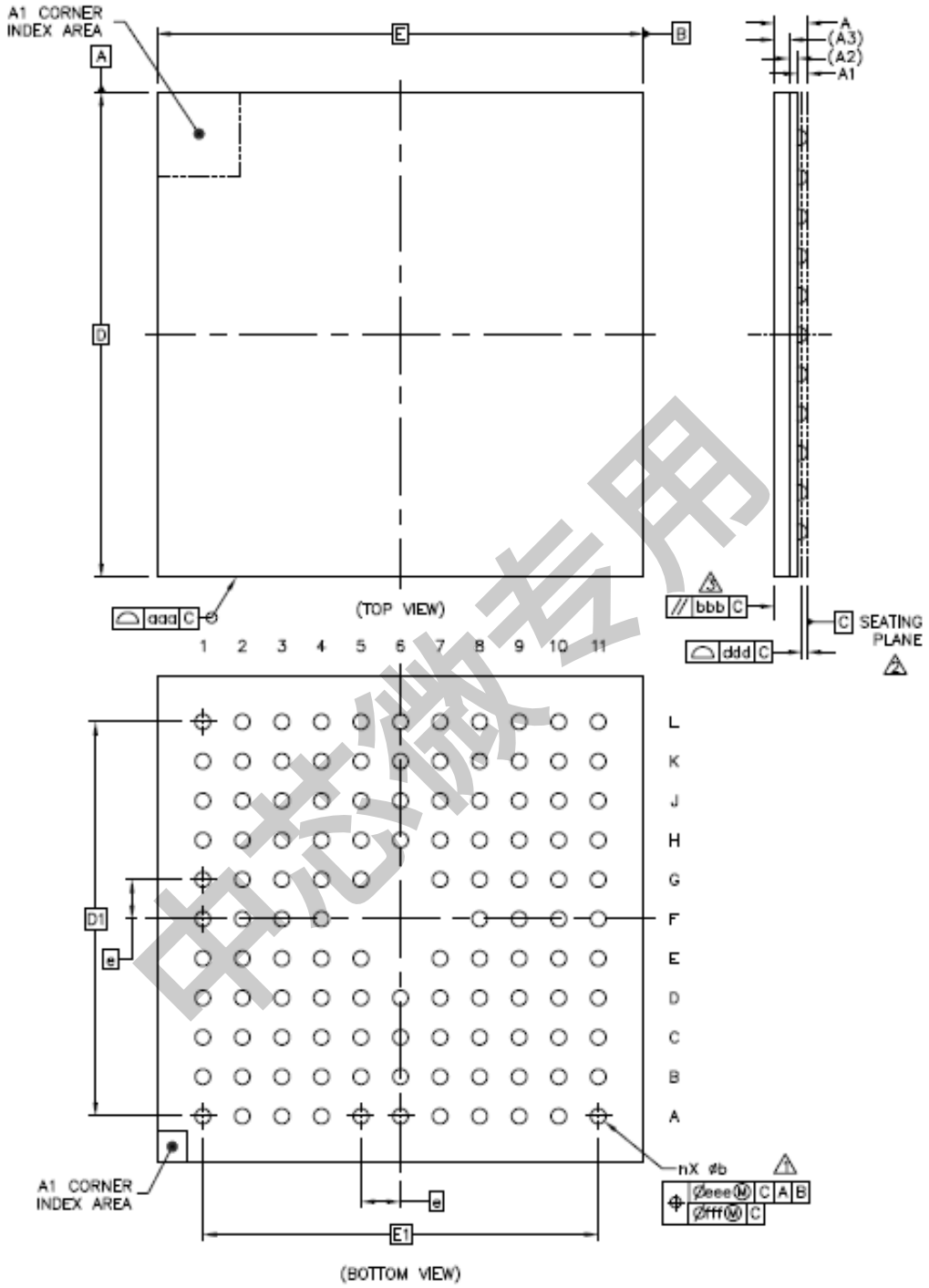
Item Name	Symbol	Millimeter		
		Min	Typ	Max
Total Thickness	A	0.7	0.75	0.8
Stand Off	A1	0	0.035	0.05
Mold Thickness	A2	----	0.55	0.57
L/F Thickness	A3		0.203 REF	
Lead Width	b	0.15	0.20	0.25
Body Size	D		8 BSC	
	E		8 BSC	
Lead Pitch	e		0.4 BSC	
EP Size	J	6.1	6.2	6.3
	K	6.1	6.2	6.3
Lead Length	L	0.35	0.4	0.45
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.1	
Coplanarity	ccc		0.08	
Lead Offset	ddd		0.1	
Exposed Pad Offset	eee		0.1	

5.2 Package Information of QFN-10x10-88L Package



Item Name	Symbol	Millimeter		
		Min	Typ	Max
Total Thickness	A	0.7	0.75	0.8
Stand Off	A1	0	0.035	0.05
Mold Thickness	A2	----	0.55	0.57
L/F Thickness	A3		0.203 REF	
Lead Width	b	0.15	0.20	0.25
Body Size	D		10 BSC	
	E		10 BSC	
Lead Pitch	e		0.4 BSC	
EP Size	J	8	8.1	8.2
	K	8	8.1	8.2
Lead Length	L	0.35	0.4	0.45
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.1	
Coplanarity	ccc		0.08	
Lead Offset	ddd		0.1	
Exposed Pad Offset	eee		0.1	

5.3 Package Information of BGA-8x8-116L Package



Item	SYMBOL	Millimeter		
		MIN	TYP	MAX
TOTAL THICKNESS	A	----	----	0.6
STAND OFF	A1	0.12	----	0.2
SUBSTRATE THICKNESS	A2	0.125 REF		
MOLD THICKNESS	A3	0.25 REF		
BODY SIZE	D	8 BSC		
	E	8 BSC		
BALL DIAMETER		0.25		
BALL OPENING		0.25		
BALL WIDTH	b	0.2	----	0.3
BALL PITCH	e	0.65		
BALL COUNT	n	116		
EDGE BALL CENTER TO CENTER	D1	6.5 BSC		
	E1	6.5 BSC		
BODY CENTER TO CONTACT BALL	SD	---- BSC		
	SE	---- BSC		
PACKAGE EDGE TOLERANCE	aaa	0.1		
MOLD FLATNESS	bbb	0.1		
COPLANARITY	ddd	0.08		
BALL OFFSET (PACKAGE)	eee	0.15		
BALL OFFSET (BALL)	fff	0.08		

5.4 Order Information

Package Type	QFN / BGA
	88Pin(10*10)/116Pin (8 * 8)
	0.8-P0.4/0.6 - P0.65
Product Name	FT5506EEG/FT5606NED/FT5616KHD/FT5816KHC

Note:

1). The last three letters in the product name indicate the package type and lead pitch and thickness.

2). The three last letter indicates the package type.
E : QFN-8*8, **N** : QFN-10*10, **K** : BGA-8*8

3). The second last letter indicates the lead pitch and thickness.
E : 0.75 - P0.4, **H**: 0.6 - P0.65

4). The last letter indicates the numbers of TX and RX.
C: 48TX-36RX , **D**: 38TX-27RX ,**G**: 32TX-20RX

T: Track Code

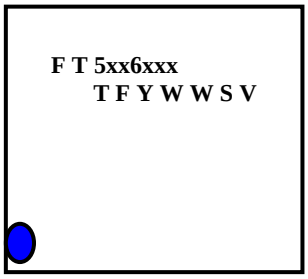
F: ”F” for Lead Free process.
”R” for Halogen Free process

Y: Year Code

WW: Week Code

S: Lot Code

V：IC Version



Product Name	Package Type	# TX Pins	# RX Pins
FT5506EEG	QFN-68L	32	20
FT5606NED	QFN-88L	38	27
FT5616KHD	BGA-116L	38	27
FT5816KHC	BGA-116L	48	36

END OF DATASHEET

联系方式

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